Hardware Scheduler Memory Arrangement
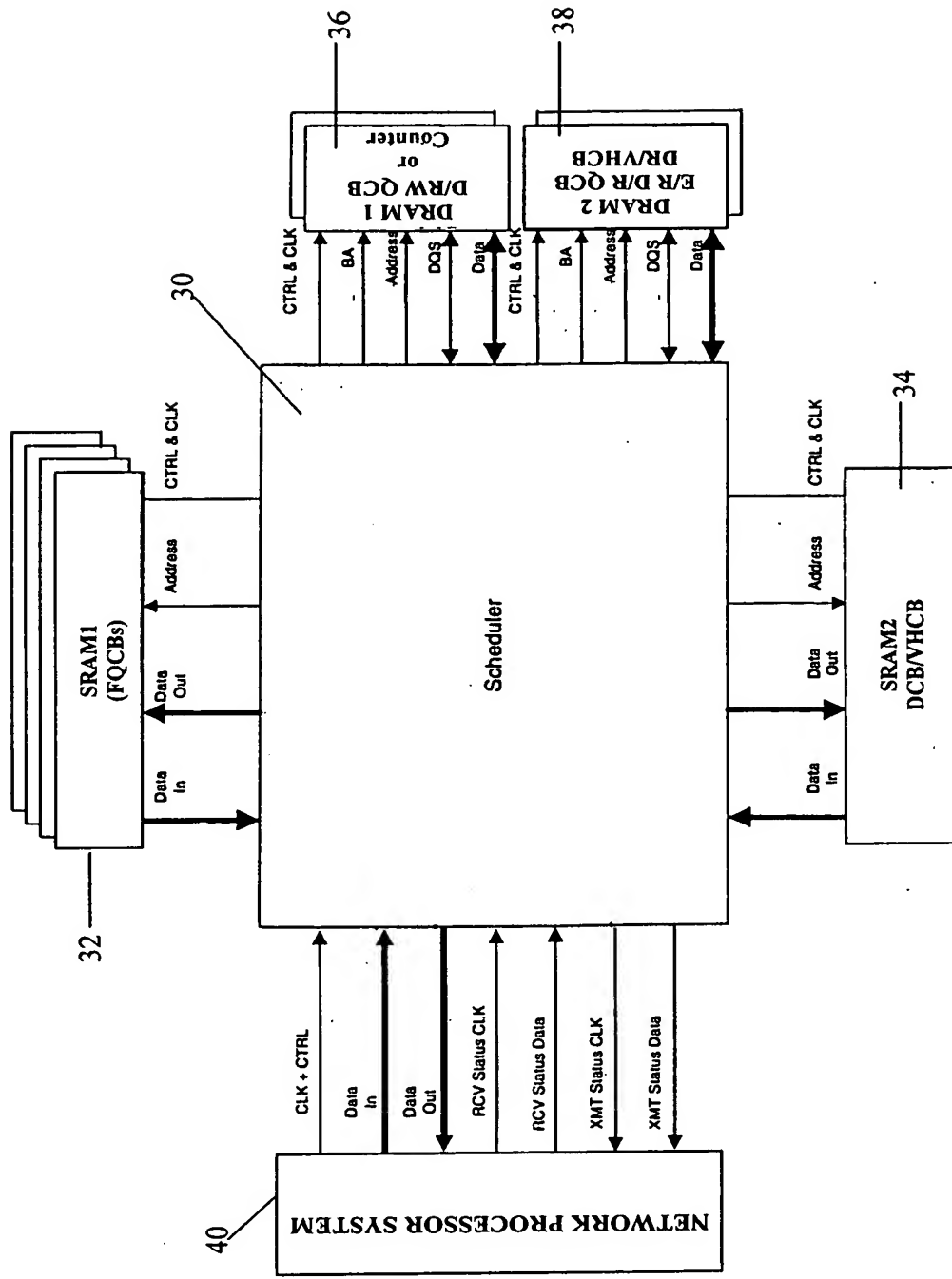

Figure 1

Hierarchical Link Resource Sharing (Variable packet size model)
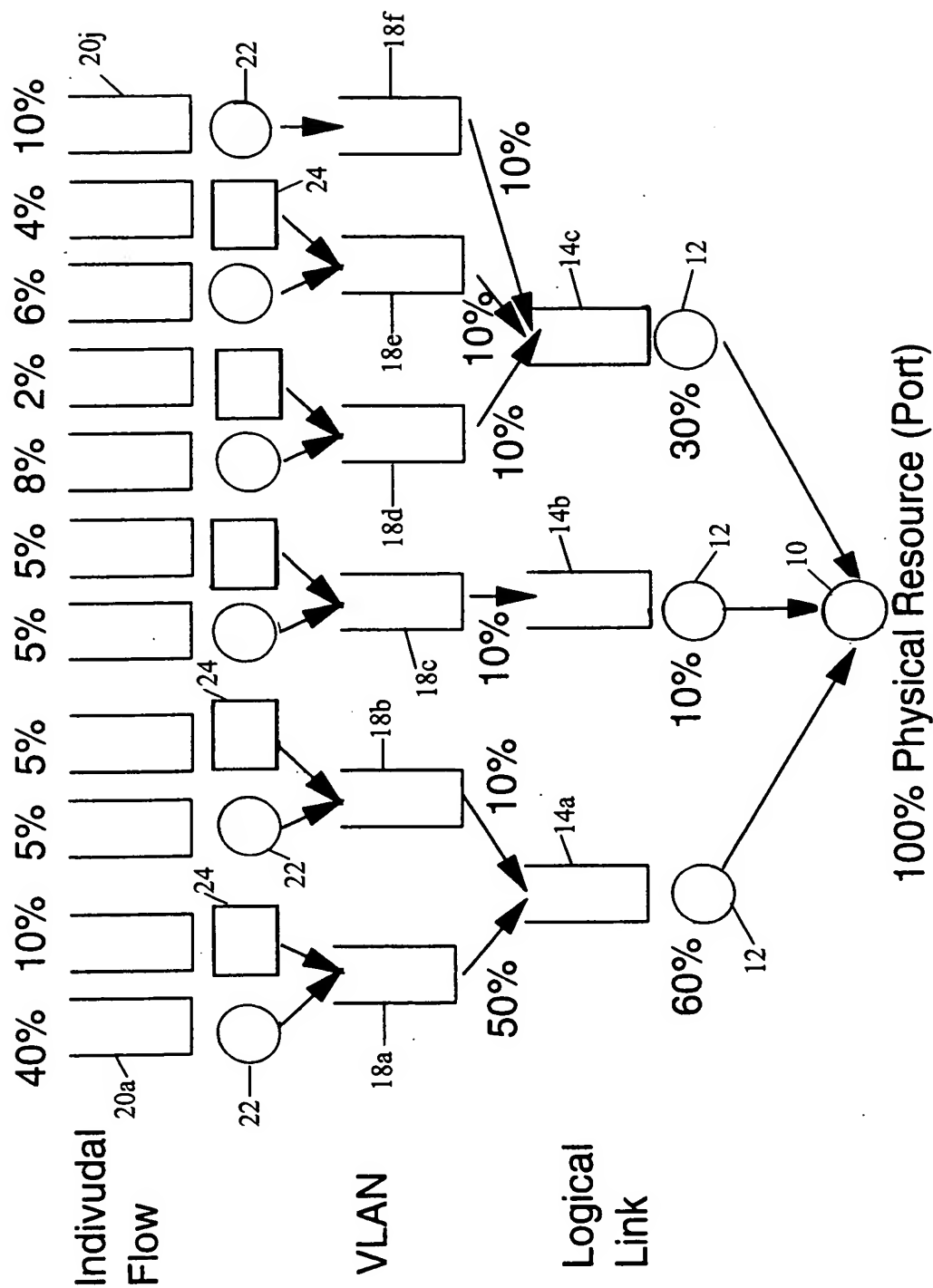

Figure 2

Scheduler Components and Scheduling Units Representation
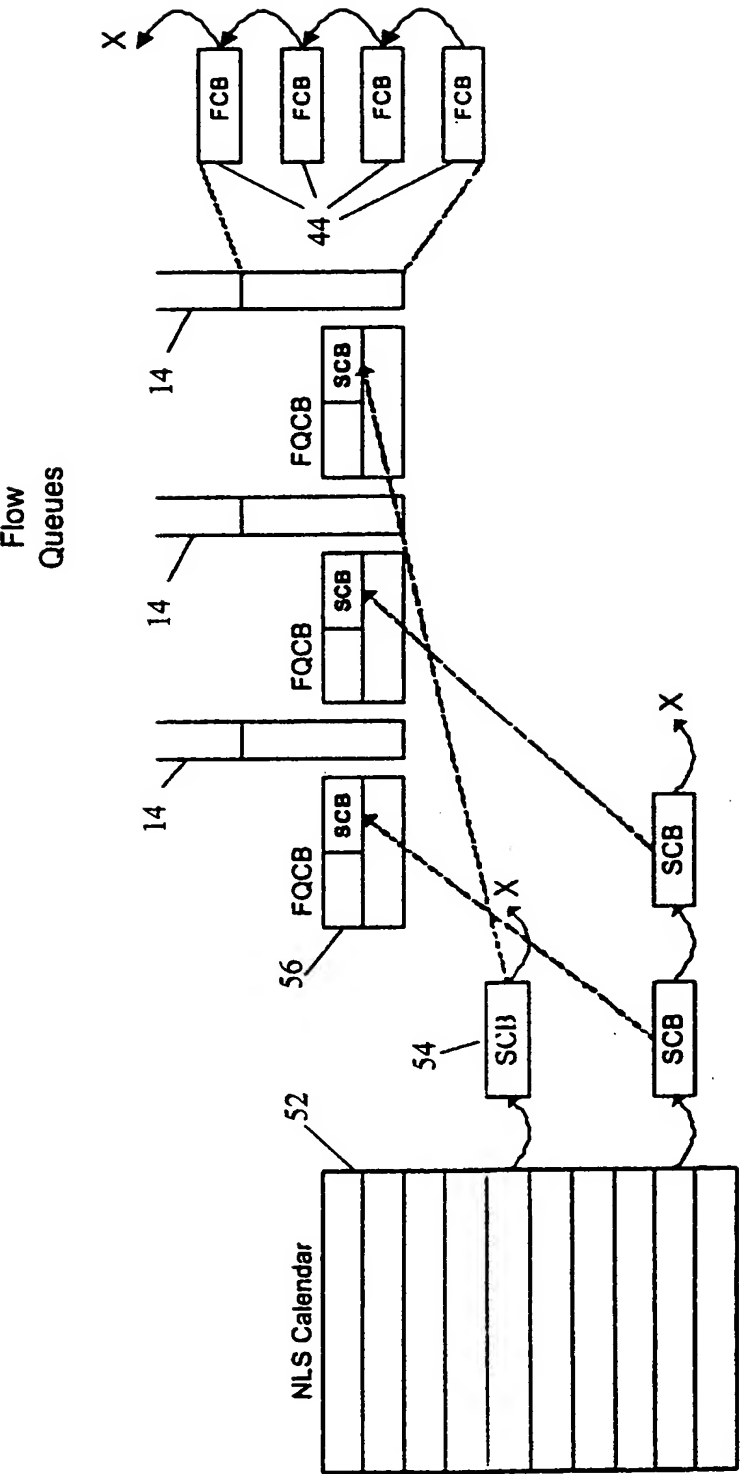
Flow
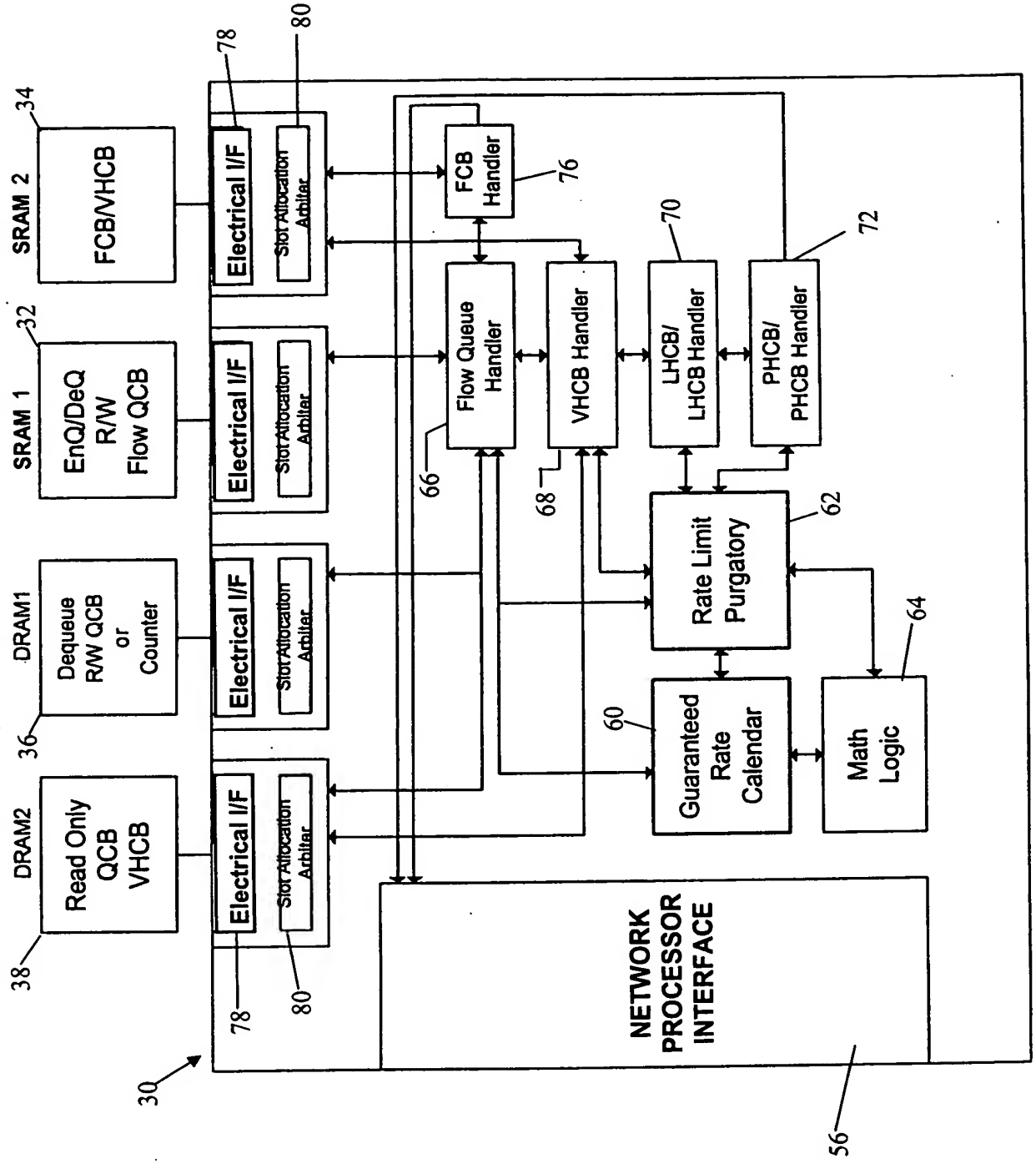Queues

Figure 3

Scheduler Functional Block Diagram

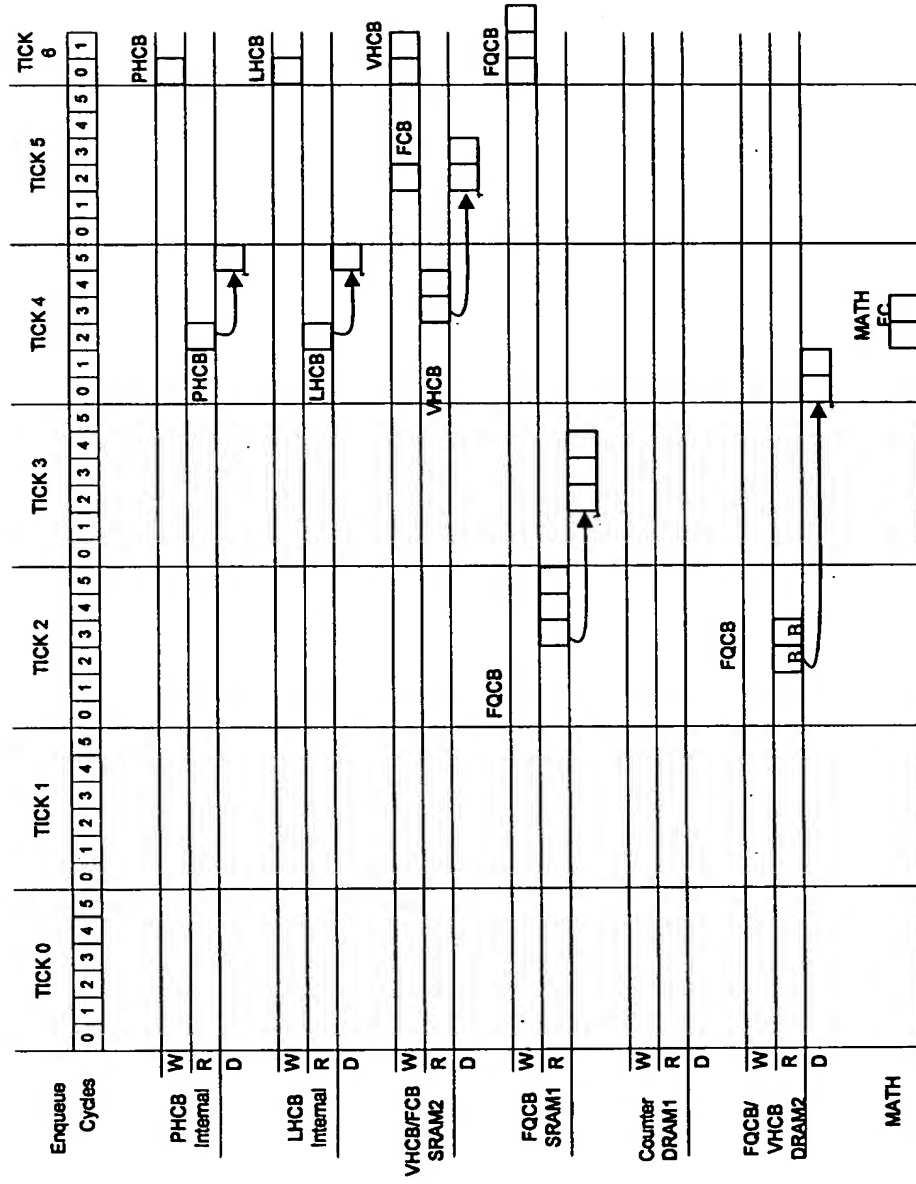Figure 4

Pipeline Design for Flow Queue Enqueue Processes

Figure 5

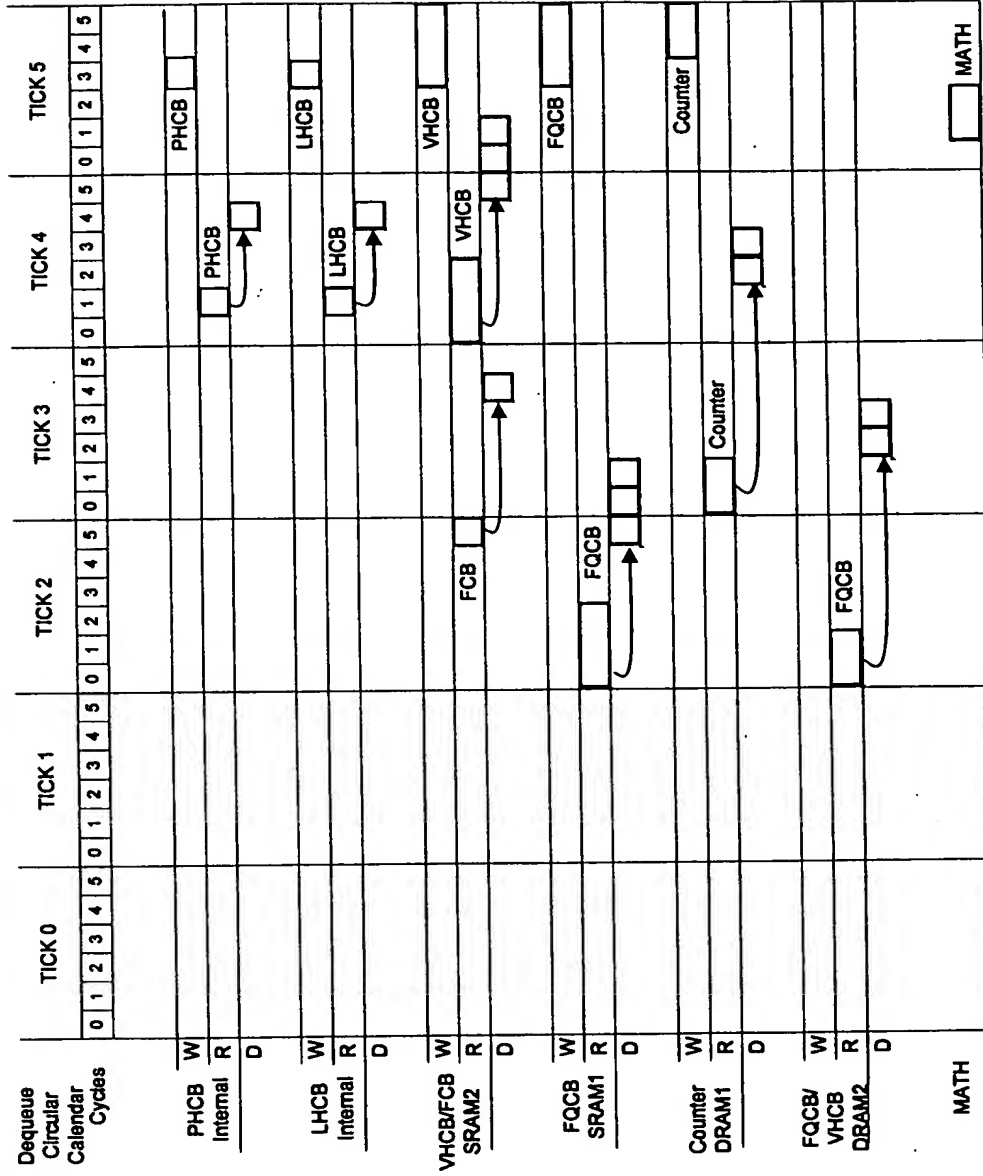Pipeline Design for Guaranteed Rate Flow Queue Dequeue Process

Figure 6

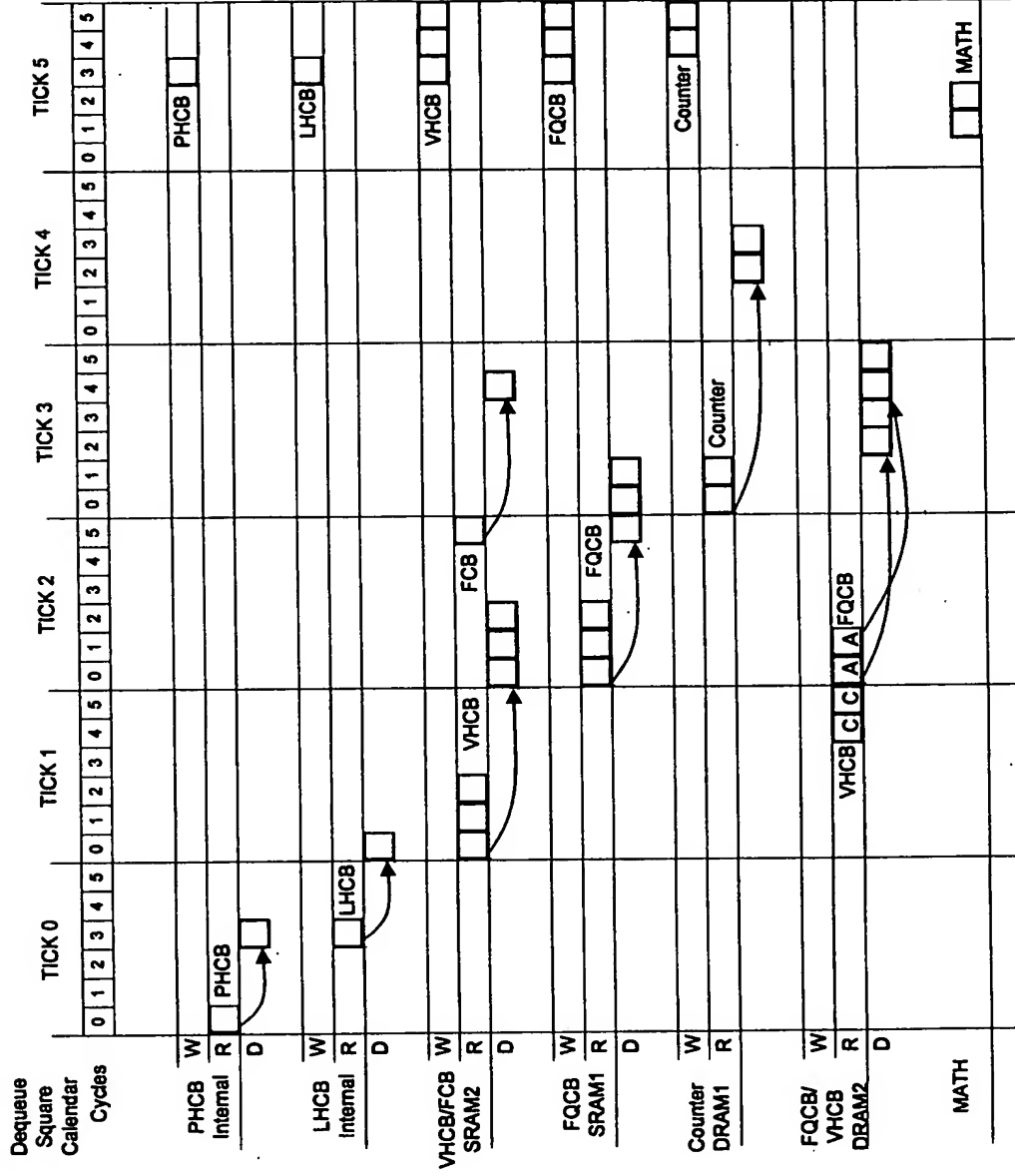Pipeline Design for Best-Effort Services Flow Queue Dequeue Processes

Figure 7
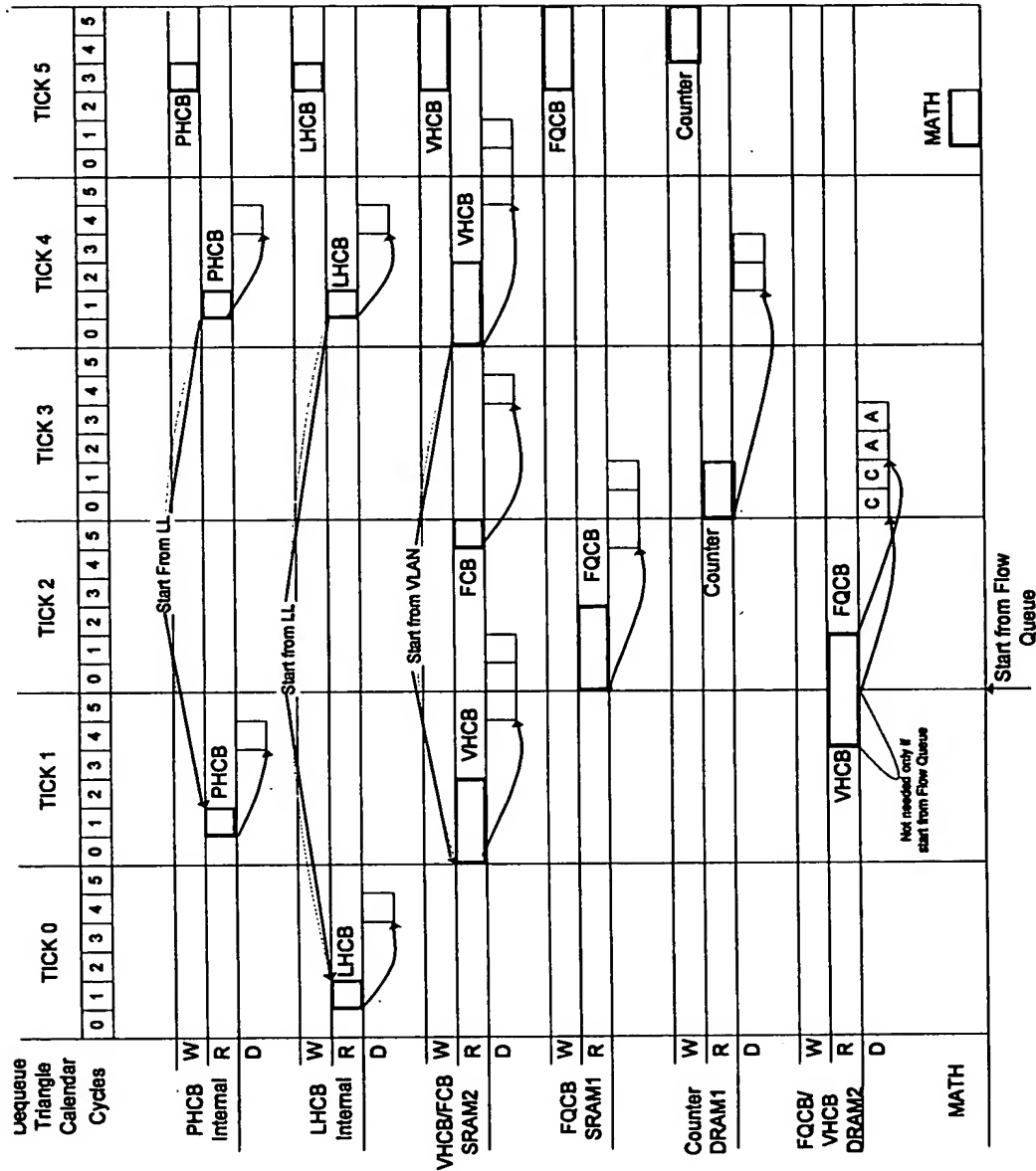
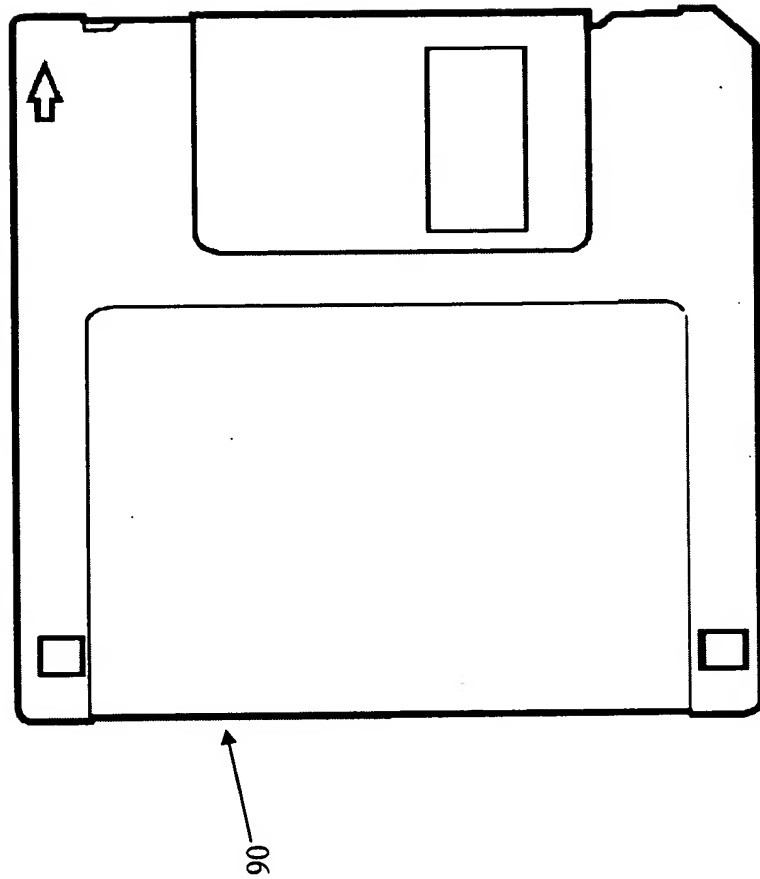Dequeue Pipeline Design for Hierarchical Access Allocation

Figure 8

90

Figure 9